



LTSSM

Recovery

PROTOTYPE

PREDICTIVE ENGINEERING

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CONCURRENT MANUFACTURING





- Recovery Link state
- Recovery requirements
- Recovery sub-state machines





- Recovery link state is entered to retain the link
- In order to retain the link last trained equalizer configurations are maintained
- TS1 and TS2 ordered sets are transmitted to synchronize the link and exchange the link configuration information

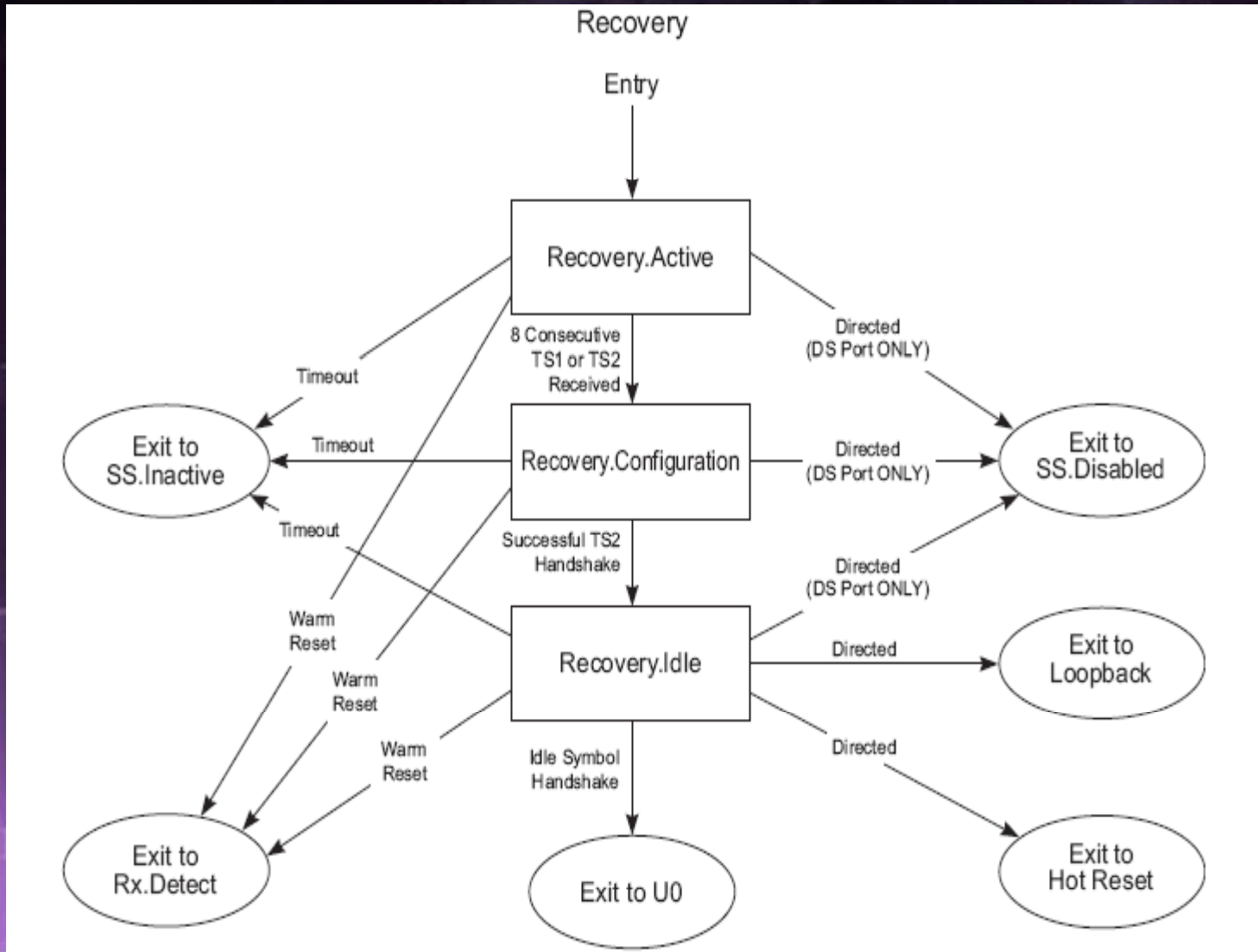
Recovery requirements

- The port shall meet the transmitter specifications
- The port shall maintain the low impedance receiver termination R_{Rx-DC}
- All header packets in Tx Header Buffer and the Rx Header Buffer shall be handled based on the requirements of flow control, error recovery and power management



Recovery Sub-State Machines

- Recovery.Active
- Recovery.Configuration
- Recovery.Idle





- Recovery.Active train the super speed link by transmitting TS1 ordered set
- Recovery.Active Requirements
- A 12-ms timer shall be started on entry to this state
- The port shall transmit TS1 ordered set in this sub-state
- The port shall train its receiver with TS1 or TS2 ordered sets



- The port shall transition to Recovery.Configuration after eight consecutive and identical TS1 or TS2 ordered sets are received
- The port shall transit to SS.inactive on following conditions
 1. Either the Ux_EXIT_TIMER or 12-ms timer times out
 2. For a downstream port, the transition to recovery is not to attempt a Hot Reset
- A downstream port shall transit to Rx.Detect when the following conditions are met
 1. Either the Ux_EXIT_TIMER or 12-ms timer times out
 2. The transition to recovery is to attempt a Hot Reset
- A downstream port shall transit to SS.Disabled when directed
- A downstream port shall transit to Rx.Detect when directed to issue Warm Reset
- An upstream port shall transit to Rx.Detect when Warm Reset is detected



- Recovery.Configuration allow two link partners to achieve super-speed handshake by exchanging TS2 ordered sets
- Recovery.Configuration Requirements
- Port shall transmit identical TS2 ordered sets and set the link configuration field in TS2 ordered sets based on following
 1. When directed, a downstream port shall set reset bit in the TS2 ordered set
 2. When directed, the port shall set Loopback bit in the TS2 ordered set
 3. When directed, the port shall set the Disabling Scrambling bit in the TS2 ordered set
- A 6-ms timer shall be started upon entry to this substate

Exit from Recovery.Configuration

- The port shall transit to Recovery.Idle after the following two conditions are met
 1. Eight consecutive and identical TS2 ordered sets are received
 2. Sixteen TS2 ordered sets are sent after receiving the first of the eight consecutive and identical TS2 ordered sets
- The port shall transit to SS.Inactive when the following conditions are met
 1. Either Ux_EXIT_TIMER or 6-ms timer times out
 2. The conditions to transition to Recovery.Idle are not met
 3. For a downstream port, the transition to Recovery is not to attempt a Hot Reset
- A downstream port shall transit to Rx.Detect on following
 1. Either Ux_EXIT_TIMER or 6-ms timer times out
 2. The transition to recovery is to attempt a Hot Reset
- A downstream port shall transit to SS.Disabled when directed
- A downstream port shall transit to Rx.Detect when directed to issue Warm Reset
- An upstream port shall transit to Rx.Detect when Warm Reset is detected



- Recovery.Idle is substate where port decodes the link configuration field defined in TS2 ordered sets received and determine next state
- Recovery.Idle Requirements
 - A 2-ms timer shall be started upon entry to this substate
 - The port shall transmit Idol symbols if the next state is U0
 - The port shall decode the link configuration field defined in the TS2 ordered sets received during Recovery.Configuration and next state
 - The port shall enable the scrambling by default if the disabling scrambling bit is not asserted in TS2 ordered sets received
 - The port shall disable the scrambling if directed or if disabling scrambling bit is asserted in TS2 ordered sets received
 - The port shall be able to receive the Header Sequence Number Advertisement from its link partner

Exit from Recovery.Idle

- The port shall transition to Loopback when directed as a Loopback Master and the port is capable of being a loopback Master
- The port shall transit to loopback as loopback slave if the loopback bit is asserted in TS2 ordered sets
- The shall transit to U0 when following two conditions are met
 1. Eight consecutive Idle symbols are received
 2. Sixteen Idle symbols are sent after receiving one Idle symbol
- The port shall transit to SS.Inactive when one of the following timers times out and conditions to transition to U0 are not met
 1. Ux_EXIT_TIMER
 2. The 2-ms timer
- A downstream port shall transit to Hot Reset when directed
- A downstream port shall transit to SS.Disabled when directed
- A downstream port shall transit to Rx.Detect when directed to issue Warm Reset
- An upstream port shall transit to Rx.Detect when Warm Reset is detected
- An upstream port shall transit to Hot Reset if the reset bit is asserted in TS2 ordered sets



Loop Back

PROTOTYPE

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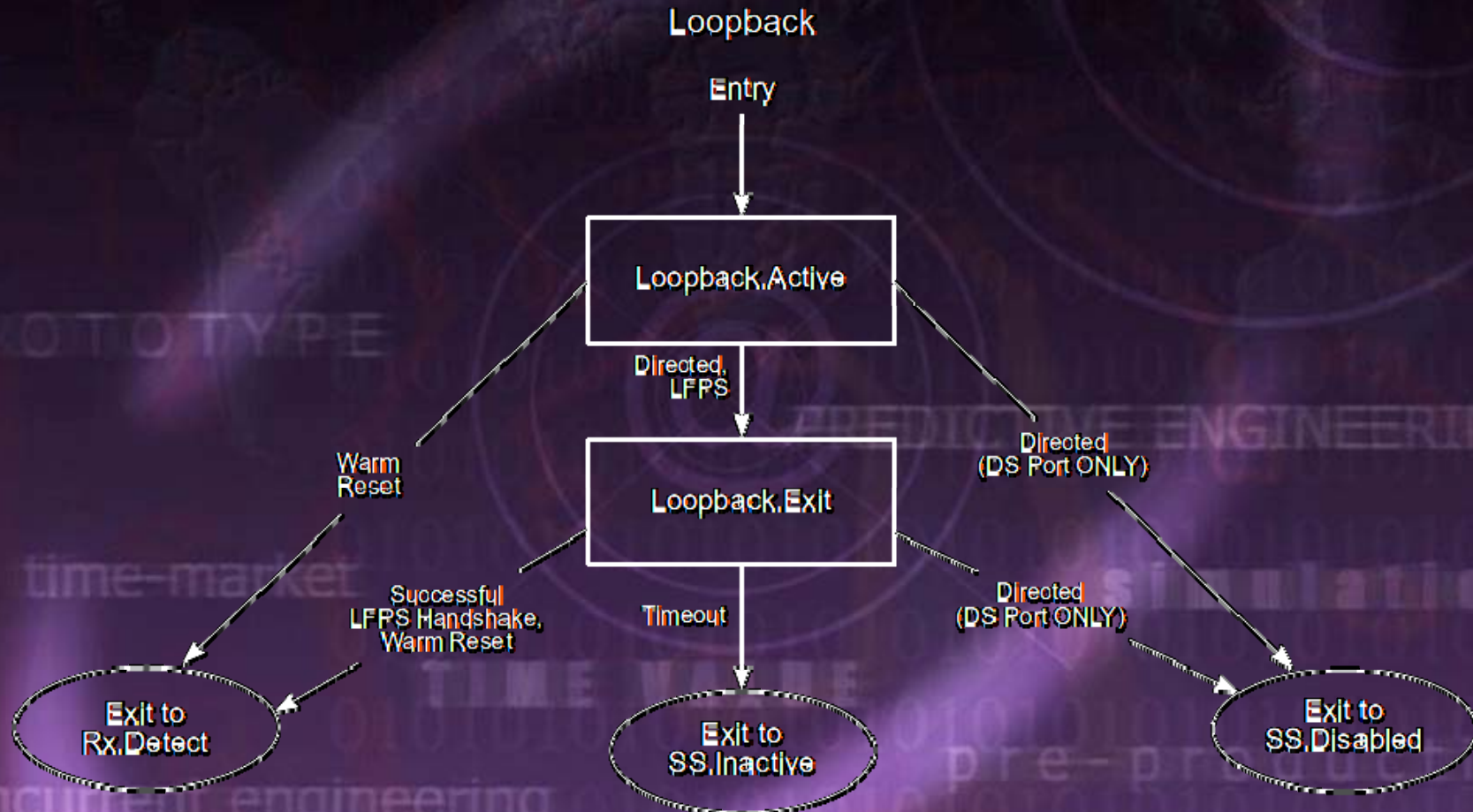
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Loopback Requirements

- Loopback is intended for test and fault isolation
- Loopback Master/Slave
 - During recovery or polling state, if TS2 ordered set is received with loopback bit asserted, it would act as a loop back slave otherwise it would be loop back master
 - Master/Slave support BERT protocol (Chapter 6)
- Loopback contains a substate machine with the following substates:
 - Loopback.Active
 - Loopback.Exit



Note: Transition conditions are illustrative only. Not all of the transition conditions are listed.

Loopback.Active



- Loopback.Active is a sub-state where the loopback test is active.
- The loopback master is sending data/commands to its loopback slave.
- The loopback slave is either looping back the data or detecting/executing the commands it received from the loopback master.



- **Exit from Loopback.Active**

- A downstream port shall transition to SS.Disabled when directed.
- A downstream port shall transition to Rx.Detect when directed to issue Warm Reset.
- An upstream port shall transition to Rx.Detect when Warm Reset is detected.
- The loopback slave shall transition to Loopback.Exit upon detection of successful Loopback LFPS exit handshake signal

Loopback.Exit



- Loopback.Exit is a substate where a loopback master has completed the loopback test and starts the exit from Loopback.
- **Loopback.Exit Requirements**
 - A 2-ms timer shall be started upon entry to this substate.
 - The LFPS transmitter and the LFPS receiver shall be enabled.
 - The port shall transmit and receive Loopback LFPS exit handshake signals



- **Exit from Loopback.Exit**

- The port shall transition to Rx.Detect upon a successful Loopback LFPS exit handshake defined in chapter 6
- The port shall transition to SS.Inactive upon the 2-ms timer timeout and the condition to transition to Rx.Detect is not met.
- A downstream port shall transition to SS.Disabled when directed.
- A downstream port shall transition to Rx.Detect when directed to issue Warm Reset.
- An upstream port shall transition to Rx.Detect when Warm Reset is detected.



Hot Reset

PROTOTYPE

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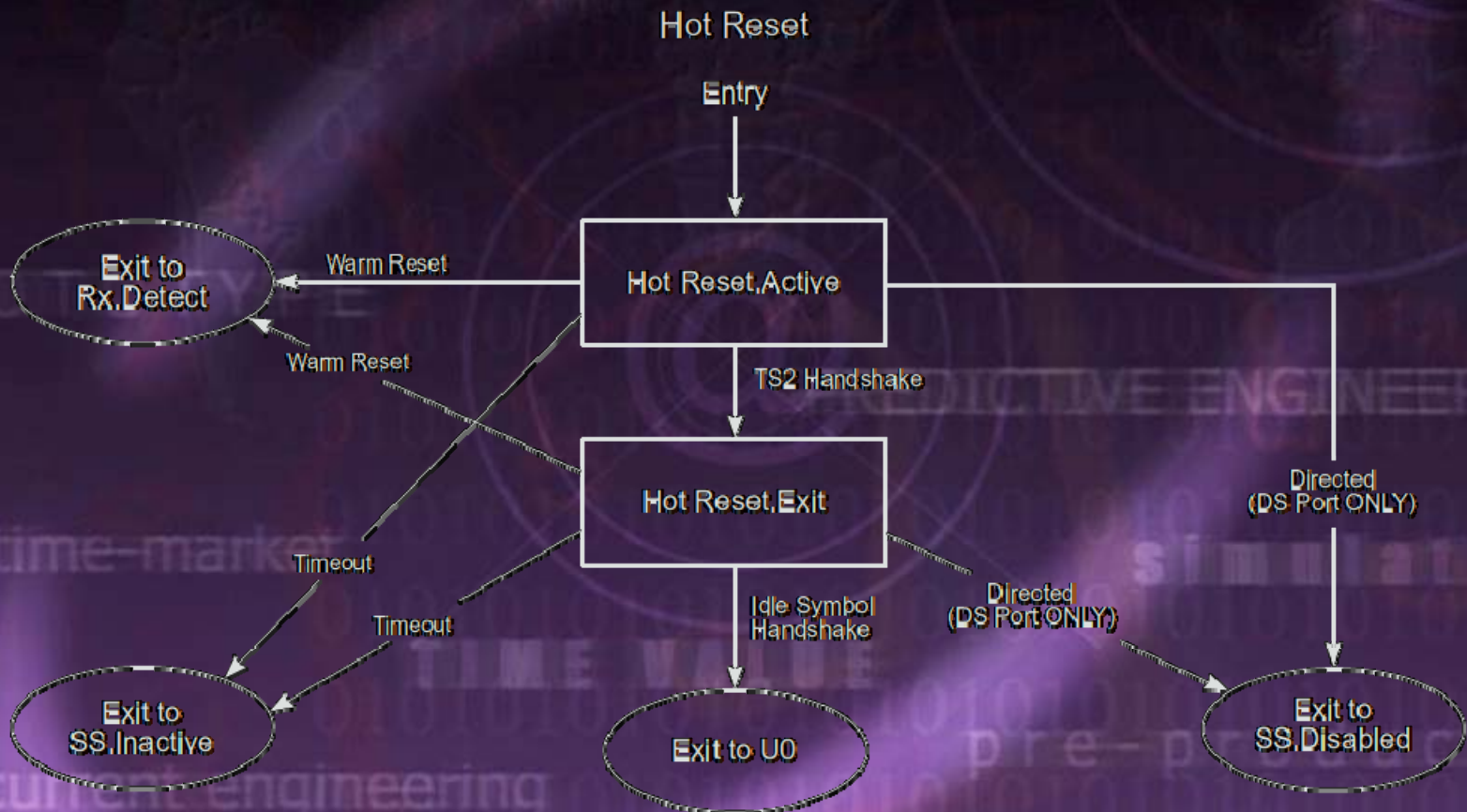
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Note: Transition conditions are illustrative only. Not all of the transition conditions are listed.

U-056

Hot Reset Link State



- Hot Reset can only be initiated by a downstream port.
- A downstream port shall reset its Link Error Count.
- The port configuration information of an upstream port shall remain unchanged.
- A downstream port shall reset its PM timers and the associated U1 and U2 timeout values to zero.



- A downstream port may be directed to reset the link in two ways, PORT_RESET”, or “BH_PORT_RESET”.
 - Port is in U0.
 - Port is in U1 or U2, it shall exit U1 or U2 using the LFPS exit handshake, transition to recovery and then transition to Hot Reset.
 - Port is in a transitory state of Polling or Recovery.
 - Port is in SS.Disabled, an Inband Reset is prohibited.

Hot Rest Sub-State



- HotReset.Active
- HotReset.Exit





- Will transition to this state.
- Downstream port will start sending TS2 order set with reset bit asserted.(min 16)
- In response to this upstream port will perform the same operation.
- Repeated until upstream port does reset and start transmitting TS2 order set with reset bit de-asserted.



- Transition to Hot Reset.Exit
 - At least 16 TS2 ordered sets with the Reset bit asserted are transmitted.
 - 2. Two consecutive TS2 ordered sets are received with the Reset bit de-asserted.
 - 3. Four consecutive TS2 ordered sets with the Reset bit de-asserted are sent after receiving one TS2 ordered set with the Reset bit de-asserted.

- Transition to SS.Inactive upon the 12-ms timer timeout.(DP)
- Transition to SS.Disabled when directed. (DP)
- transition to Rx.Detect when directed to issue Warm Reset.(Both)



- The port shall transmit idle symbols.
- A 2-ms timer shall be started upon entry to this substate.
- The port shall be able to receive the Header Sequence Number Advertisement from its link partner.



- Transition to U0
 - 1. Eight consecutive Idle Symbols are received.
 - 2. Sixteen Idle Symbols are sent after receiving one Idle Symbol.
- Transition to SS.Inactive upon the 2-ms timer timeout.(DP)
- Transition to SS.Disabled when directed.(DP)
- Transition to Rx.Detect when directed to issue Warm Reset.(Both)